



Sheet 1 of 3

FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		Attorney Docket No.: L&L-I0232	Applic. No. 10/047,013
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))		Applicant Wolfgang Rösner et al.	
		Filing Date January 16, 2002	Group Art Unit 2811

U.S. PATENT DOCUMENTS

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
PG	A	5,714,766	02/03/98	Chen et al.			
	B						
	C						
	D						
	E						
	F						
	G						
	H						
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FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL YES	NO
PG	J	196 32 835 C1	04/02/98	Germany				X
PG	K	0 843 361 A1	05/20/98	Europe			X	
	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

PG	O	H.I. Liu et al.: "Self-limiting oxidation for fabricating sub-5 nm silicon nanowires", Appl. Phys. Lett., Vol. 64, No. 11, March 14, 1994, pp. 1383-1385
PG	P	Harald Gossner et al.: "Vertical Si-Metal-Oxide-Semiconductor Field Effect Transistors with Channel Lengths of 50 nm by Molecular Beam Epitaxy", Jpn. J. Appl. Phys., Vol. 33, 1994, pp. 2423-2428

EXAMINER *RL* DATE CONSIDERED *04/10/02*

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609;
 Draw line through citation if not in conformance and not considered. Include copy of this form with
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APR 08 2002

Sheet 2 of 3

FORM PTO-1449 (SUBSTITUTE)

U.S. DEPARTMENT OF COMMERCE
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EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A						
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	D					1 C 2000	1
	E					2000	2
	F					2000	3
	G					2000	4
	H					2000	5
	I					2000	6

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES NO
	J						
	K						
	L						
	M						
	N						

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

<i>RB</i>	O	Lothar Risch et al.: "Vertical MOS Transistors with 70 nm Channel Length", IEEE Transactions on Electron Devices, Vol. 43, No. 9, September 1996, pp. 1495-1498
<i>FB</i>	P	Hiroshi Fukuda et al.: "Fabrication of silicon nanopillars containing polycrystalline silicon/insulator multilayer structures", Appl. Phys. Lett., Vol. 70, No. 3, January 20, 1997, pp. 333-335

EXAMINER	<i>RBL</i>	DATE CONSIDERED
		<i>04/20/02</i>

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EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A						
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	D						
	E						
	F						
	G						TC 2600
	H						ALL P
	I						LCR - L

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL YES	TRANSL NO
	J							
	K							
	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

P6	O	Hiroshi Mizuta et al.: "High-speed single-electron memory: cell design and architecture", XP-002151823, IEEE 1998, pp. 67-72
	P	
EXAMINER		DATE CONSIDERED 04/01/03

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